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TI - MONITORING SYSTEM FOR FAULT OF MASTER MICROPROCESSOR
IN - WAKAHARA YASUSHI; ISOGAWA YOUICHI; MAEDA MASAHITO
PA - KOKUSAI DENSHIN DENWA CO LTD; NIPPON ELECTRIC CO
EC - G06F11/00B1
IC - G06F11/20 ; G06F11/30 ; G06F15/16
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IN - WAKAHARA YASUSHI; others: 02
PA - KOKUSAI DENSHIN DENWA KK; others: 01
TI - MONITORING SYSTEM FOR FAULT OF MASTER MICROPROCESSOR
AB - PURPOSE:To determine a new master microprocessor even if a new master microprocessor and its fault detecting circuit are faulty, by providing a timer which monitors the normalcy of the new master microprocessor.
- CONSTITUTION:When a microprocessor 11 as a master microprocessor becomes faulty, fault information is reported to a fault information gathering circuit 2 of a common controlling part 1. The circuit 2 starts a timer circuit 3 and a master microprocessor determining circuit 4. The circuit 4 determines a microprocessor 12 as a new master microprocessor and reports it to microprocessors 11-1n. Microprocessors 11-1n detect through common bus interface circuits 31-3n that the new master microprocessor is changed to the processor 12. In this case, if the processor 12 is faulty or not mounted, the time-out of the circuit 3 occurs because the stop indication of the circuit 3 is not generated, and the circuit 4 is started to instruct the circuit 4 to determine a new master microprocessor again.
I - G06F11/30 ;G06F11/20 ;G06F15/16